

*Commissioner for Patents
Amendment dated March 30, 2005
Response to Office Action dated December 29, 2004
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*Serial No.: 10/054542
Art Unit: 3729
Examiner: Trinh
Docket No. RPS9 2000 0103 US2*

Amendments to the Abstract:

Please replace the original Abstract with the following new Abstract:

A method for reducing the impedance of a reference path in a printed circuit board includes forming a printed circuit board having a plurality of conductive layers including first, second, third, and fourth layers. The printed circuit board includes two or more vias interconnecting two or more of the conductive layers. A first via is part of a signal path configured to carry a signal from the first layer to the second layer. A second via is part of a reference path configured to carry said signal from a third layer to a fourth conductive layer. The method further includes embedding an electrical component, such as a capacitor, in the second via between two of the conductive layers.